In the Claims:

Please amend claim 30 as follows:

1. (Previously Presented) A processor having a set of operations made up of all the operations that are executable by the processor, each of said operations being specified by an instruction received by the processor in one of first and second external instruction formats, F1 and F2, and each of said external formats, F1 and F2, having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each of said opcode bits in one of said external formats, F1 and F2, that has an individually corresponding opcode bit in the other one of said external formats, F1 and F2, being a common F1-F2 opcode bit in the format concerned so that each of said external formats, F1 and F2, has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$, the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which employs the opcode bits to translate each instruction received in at least one of said external formats F1 and F2 into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

wherein:

all of the operations of said set of operations that are specifiable in said second external format F2 have distinct opcodes in said second external format F2; and

for every one of the operations of said set of operations that is specifiable both in said first and second external formats, all the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 are purposefully identical to one another.

2. (Cancelled)

3. (Previously Presented) A processor as claimed in claim 1, also adapted to receive instructions specifying operations of said set of operations in a third external instruction format F3, said third external format F3 having one or more opcode bits in which an opcode, specifying the operation to be executed, appears,

wherein:

each of said opcode bits in one of said external formats, F2 and F3, that has an individually corresponding opcode bit in the other one of the formats F2 and F3 is a common F2-F3 opcode bit in the format concerned so that each of said external formats F2 and F3 has, among its said one or more opcode bits, the same number C' of common F2-F3 opcode bits in total, where $C' \geq 1$,

said at least one execution unit receives instructions in at least one of first and second internal instruction formats G1 and G2 and executes the operations specified thereby;

for each operation of said set of operations that is specifiable both in said first and second external formats, said at least one instruction translation unit translates the instruction specifying the operation in either said first or second external format F1 or F2 into said first internal format G1, and for each operation of said set of operations that is specifiable both in said second and third external formats, said at least one instruction translation unit translates an instruction specifying the operation in either said second or third external format F2 or F3 into said second internal format G2; and

for every one of the operations of said set of operations that is specifiable both in said second and third external formats, F2 and F3, all the mutually-corresponding common F2-F3 opcode bits in the two external formats F2 and F3 are purposefully identical to one another.

4. (Cancelled)

5. (Original) A processor as claimed in claim 1, being a VLIW processor, wherein one external format is a scalar instruction format used for scalar instructions, and another external format is a VLIW instruction format used for VLIW instructions.

6. (Original) A processor as claimed in claim 1, being a VLIW processor, wherein the external formats are or comprise two different VLIW formats.

7. (Original) A processor as claimed in claim 6, wherein the two different VLIW formats are used in different respective instruction slots of a VLIW instruction parcel.

8. (Original) A processor as claimed in claim 6, wherein at least one instruction slot of a VLIW instruction parcel uses the two different VLIW formats.

9. (Original) A processor as claimed in claim 1, wherein one external format has an instruction width different from that of another external format.

10. (Previously Presented) A processor as claimed in claim 1, wherein:

said at least one translation unit performs a predetermined translation operation to translate each said external-format opcode into a corresponding internal-format opcode.

11. (Original) A processor as claimed in claim 10, wherein said translation operation involves selecting and/or permuting bits amongst said preselected opcode bits in the external-format instruction.

12. (Original) A processor as claimed in claim 10, wherein the translation operation is independent of the external-format opcode.

13. (Original) A processor as claimed in claim 12, wherein the translation unit identifies the internal format into which each external-format instruction is to be translated, and carries out said translation operation according to the identified internal format.

14. (Currently Amended) A machine-readable storage medium storing instructions to be executed by a processor, each said instruction being represented

in one of first and second external instruction formats, F1 and F2, of the processor, and each instruction specifying one operation of a set of operations made up of all the operations executable by the processor and causing the processor to execute the operation specified by the instruction , and each of said external formats, F1 and F2, having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each of said opcode bits in one of said external formats, F1 and F2, that has an individually corresponding opcode bit in the other one of said external formats, F1 and F2, being a common F1-F2 opcode bit in the format concerned so that each of said external formats, F1 and F2, has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$, wherein:

all of the operations of said set of operations that are specifiable in said second external format F2 have distinct opcodes in said second external format F2; and

for every one of the operations of said set of operations that is specifiable both in said first and second external formats , all the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 are purposefully identical to one another, whereby a

translation process performed by the processor to translate the external-format instructions into corresponding instructions in an internal format used by an execution unit within the processor can be independent of the opcodes.

15. (Previously Presented) A method of encoding instructions for a processor in at least first and second external instruction formats, F1 and F2, of the processor, each said instruction in one of said external formats specifying one operation of a set of operations made up of all the operations executable by the processor and causing the processor to execute the specified operation, and each of said external formats, F1 and F2, having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each of said opcode bits in one of external formats, F1 and F2, that has an individually corresponding opcode bit in the other one of said external formats, F1 and F2, being a common F1-F2 opcode bit in the format concerned so that each of said external formats, F1 and F2, has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$,

said method comprising:

encoding all of the operations of said set of operations that are specifiable in said second external format F2 with distinct opcodes in said second external format F2;

for every one of the operations of said set of operations that is specifiable both in said first and second external formats, F1 and F2, encoding the respective opcodes of the operations in said first and second external formats so that all the mutually-corresponding

common F1-F2 opcode bits in the two external formats F1 and F2 are purposefully identical to one another, whereby a translation process performed by the processor to translate the external-format instructions into corresponding instructions in an internal format used by an execution unit within the processor can be independent of the opcodes.

16-29. (Cancelled)

30. (Currently Amended) A propagated signal embodying instructions to be executed by a processor, each said instruction being ~~stored~~ represented in one of first and second external instruction formats, F1 and F2, of the processor and each instruction specifying one operation of a set of operations made up of all the operations executable by the processor and causing the processor to execute the operation specified by the instruction, and each of said external formats, F1 and F2, having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each of said opcode bits in one of said external formats, F1 and F2, that has an individually corresponding opcode bit in the other one of said external formats, F1 and F2, being a common F1-F2 opcode bit in the format concerned so that each of said external formats, F1 and F2, has, among its said one or more opcode bits, the same number C of common F1-F2 opcode bits in total, where $C \geq 1$,

wherein:

all of the operations of said set of operations that are specifiable in said second external format F2 have distinct opcodes in said second external format F2; and

for every one of the operations of said set of operations that is specifiable both in said first and second external formats , all the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 are purposefully identical to one another, whereby a translation process performed by the processor to translate the external-format instructions into corresponding instructions in an internal format used by an execution unit within the processor can be independent of the opcodes.

31. (Previously Added) A processor as claimed in claim 1, wherein the mutually-corresponding common F1-F2 opcode bits in the two external formats F1 and F2 both have the same bit position.

32. (Previously Added) A processor adapted to receive instructions in one of first and second external instruction formats, each instruction specifying one of a plurality of first operations executable by the processor or one of a plurality of second operations executable by the processor, and each said external format having one or more opcode bits in which an opcode, specifying the operation to be executed, appears, and each bit position at which the first and second external formats both have respective opcode bits is a common bit position;

the processor comprising:

at least one execution unit which receives instructions in an internal instruction format and executes the operations specified thereby; and

at least one instruction translation unit which employs the opcode bits to translate each

instruction received in at least one of said external formats into such an instruction in said internal format, the internal-format instruction specifying the same operation as the external-format instruction;

wherein:

each said first operation is specifiable in both said first and second external formats, and each said second operation is specifiable in said second external format;

all said first operations and all second operations have distinct opcodes in said second external format; and

for every one of the first operations which the processor is capable of executing, the first and second external formats have identical opcode bits in each said common bit position.

33. (New) The method of claim 15 comprising storing the instructions on a storage medium.